ABSTRACT

Methods and tools for detecting and correcting problems arising in the configuration process of a programmable logic device are described. An analyzer is used to aid a user in debugging the configuration process. The analyzer can access the programmable logic device through a boundary scan architecture such as JTAG. The analyzer can step through the configuration process, capturing the data received by the programmable logic device at each step, and compare that captured data with expected data. Mismatches can indicate errors in the configuration process, and the analyzer can help a user correct such errors.